58

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,377	07/27/2001	Chi-Lie Wang	3COM 3655-1	7618

22470 7590 02/23/2005

HAYNES BEFFEL & WOLFELD LLP
P O BOX 366
HALF MOON BAY, CA 94019

EXAMINER	
FAROOQ, MOHAMMAD O	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,377	WANG ET AL.	
	Examiner	Art Unit	
	Mohammad O. Farooq	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-12,16-23 and 27-33* is/are rejected.

7)☒ Claim(s) *2-4,13-15 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/27/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 5, 8-11, 12, 16, 19-22, 23, 27 and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benson et al. U.S. Pat. No. 6,026,090, in view of Yamanaka et al. U.S. Pat. No. 5,953,341.

2. As to claim 1, Benson et al. teach system, comprising:

a host processor (i.e. host; item 108, fig. 2), and

a network interface coupled to the host processor and to a network (item 114, fig. 2), the network interface comprising:

a first port that receives data from the host processor (item 118, fig. 2);

a second port that transmits data to the network (item 140, fig. 2);

a memory that stores data packets received by the first port, the memory being coupled to the first port and to the second port (item 120, fig. 2);

and a control circuit that manages the memory as a plurality of queues, including logic to place a packet received from the host into one of the plurality of queues, and logic to service packets in the plurality of queues (item 126, fig. 2).

Benson et al. do not teach priorities. Yamanaka et al. teach priorities (col. 1, lines 40-60). However, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Benso et al. and Yamanaka et al. because that would provide a contention control circuit capable of guaranteeing temporal order (col. 2, lines 45-58).

3. As to claim 5, Benson et al. teach system, further comprising logic in the network interface to execute a security process on packets in one of the plurality of queues (i.e. via transfer controller; item 208; fig. 9).

4. As to claim 8, Benson et al. teach system, wherein the packets include frame start headers (e.g. ATM packet), and said quality of service parameters comprises codes (inherent) in the frame start headers (see fig. 4).

5. As to claim 9, Benson et al. teach system, wherein said plurality of queues have statically allocated space in said memory (see fig. 5).

6. As to claim 10, Benson et al. teach system, wherein said plurality of queues include first, second and third queues, and said memory includes a first storage array for the first queue, a second storage array for the second queue, and a third storage array for third queue, and wherein said first, second and third storage arrays have respective inputs coupled to said logic to place a packet in one of the plurality of queues, and respective outputs, wherein said logic to service packets in the plurality of queues includes a multiplexer (col. 10, lines 29-40) coupled to the outputs of the first, second and third storage arrays (fig. 5,9 and 12).

7. As to claim 11, Benson et al. teach system, wherein at least one of the queues in the plurality of queues comprises a first-in-first-out FIFO queue (item 210, fig. 9).

8. As to claim 12, Benson et al. teach apparatus, comprising:

managing memory (item 126, fig. 2) in the network interface apparatus (item 114, fig. 2) as a plurality of queues, including placing packet received from the host processor into one of the plurality of queues, and servicing packets in the plurality of queues (see fig. 2).

Benson et al. do not teach priorities. Yamanaka et al. teach priorities (col. 1, lines 40-60). However, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Benso et al. and Yamanaka et al. because that would provide a contention control circuit capable of guaranteeing temporal order (col. 2, lines 45-58).

9. As to claim 23, Benson et al. tech integrated circuit, comprising:

a first port that receives data from the host processor (item 118, fig. 2);

a second port that transmits data to the network (item 140, fig. 2);

a memory that stores data packets received by the first port, the memory being coupled to the first port and to the second port (item 120, fig. 2); and

a control circuit that manages the memory as a plurality of queues, including logic to place a packet received from the host into one of the plurality of queues, and logic to service packets in the plurality of queues out the second port (item 126, fig. 2).

Benson et al. do not teach priorities. Yamanaka et al. teach priorities (col. 1, lines 40-60). However, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Benso et al. and Yamanaka et al. because that would provide a contention control circuit capable of guaranteeing temporal order (col. 2, lines 45-58).

10. Claims 16 and 19-22 are method claims of apparatus claims 5 and 8-11. Benson et al. and Yamanaka et al. in combination teach apparatus as set forth in claims 5 and 8-11. Therefore, Benson et al. and Yamanaka et al. also teach method as set forth in claims 16 and 19-22.

11. Claims 27 and 30-33 have similar limitations as apparatus claims 5 and 8-11. Benson et al. and Yamanaka et al. in combination teach apparatus as set forth in claims 5 and 8-11. Therefore, Benson et al. and Yamanaka et al. also teach apparatus as set forth in claims 27 and 30-33.

12. Claims 6,7,17,18, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benson et al. U.S. Pat. No. 6,026,090, in view of Yamanaka et al. U.S. Pat. No. 5,953,341 further in view of Aguilar et al. U.S. Pat. No. 6,199,137.

13. As to claims 6 and 7, neither Benson et al. nor Yamanaka et al. teach Ethernet and Inifiniband protocol.

Aguilar et al. teach Ethernet and Infiniband protocol (col. 2, lines 61-65). However, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the combination of Benson et al. and Yamanaka et al. with Aguilar et al. because that would provide increased data flow between peripheral devices and a compute platform (col. 2, lines 61-67).

14. Claims 17 and 18 are method claims of apparatus claims 6 and 7. Benson et al., Yamanaka et al. and Aguilar et al. in combination teach apparatus as set forth in claims 6 and 7. Therefore, Benson et al., Yamanaka et al. and Aguilar et al. in combination also teach method as set forth in claims 17 and 18.

15. Claims 28 and 29 have similar limitations as apparatus claims 6 and 7. Benson et al., Yamanaka et al. and Aguilar et al. in combination teach apparatus as set forth in claims 6 and 7. Therefore, Benson et al., Yamanaka et al. and Aguilar et al. in combination also teach apparatus as set forth in claims 28 and 29.

Allowable Subject Matter

16. Claims 2-4,13-15 and 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad O. Farooq whose telephone number is (571) 272-4144. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (571) 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mohammad O. Farooq
February 14, 2005